



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,787	11/26/2003	Harry Hedler	543822002200	4141
25227	7590	03/10/2006		
MORRISON & FOERSTER LLP 1650 TYSONS BOULEVARD SUITE 300 MCLEAN, VA 22102			EXAMINER PERKINS, PAMELA E	
			ART UNIT 2822	PAPER NUMBER

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/721,787

Applicant(s)

HEDLER ET AL.

Examiner

Pamela E. Perkins

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 December 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
4a) Of the above claim(s) 1-7 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 8-10 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 20 December 2005. Claims 1-10 are pending; claims 1-7 have been withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henle et al. (4,266,282) in view of Kinsman (6,380,630).

Henle et al. disclose a method for producing semiconductor components where electrical lines (12/57) are printed on main sides semiconductor chips (10/50) such that the lines (12/57) run from contact points of the semiconductor chips (10/50) beyond lower edges of the main sides onto base sides of the semiconductor chips (10/50); and fitting the chip on a carrier board (11/65) such that main planes of the semiconductor chips (10/50) run perpendicular to the carrier board (11/65) (Fig. 1, 7A & 7b; col. 3, lines 36-47; col. 7, lines 54-66; col. 8, lines 20-31).

Henle et al. do disclose producing a chip composite by adhesively bonding together non-printed main sides of two semiconductor chips.

Kinsman discloses a method for producing semiconductor components including producing a chip composite (10) by adhesively bonding together non-printed main sides of two semiconductor chips (12a, 12b); and fitting the chip composite (10) on a carrier board (40) such that main planes of the semiconductor chips (12a, 12b) run perpendicular to the carrier board (40) (Fig. 1 & 3b; col. 4, lines 52-65).

Since Henle et al. and Kinsman are both from the same field of endeavor, a method for producing semiconductor components, the purpose disclosed by Kinsman would have been recognized in the pertinent art of Henle et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Henle et al. by producing a chip composite by adhesively bonding together non-printed main sides of two semiconductor chips as taught by Kinsman to create a device with low impedance (col. 3, lines 11-15).

Referring to claim 9, Kinsman discloses introducing an adhesive (13) between the main sides of the semiconductor chips (12a, 12b); and bringing together the semiconductor chips (12a, 12b) in an adhesive bonding mold such that an at least partial encapsulation of the chip composite (10) is produced (fig. 1; col. 4, lines 52-65).

Referring to claim 10, Henle et al. disclose wherein the fitting of the chip (10/50) comprises production of soldered connections between the printed lines (12/57) and contact areas (13) of the carrier board (11/57) (col. 3, lines 36-47).

Response to Arguments

Applicant's arguments filed 20 December 2005 have been fully considered but they are not persuasive. As stated above, Henle et al. in view of Kinsman disclose the semiconductor components as described in claims 8-10.

In response to the applicant's arguments, the applicant argues Henle et al. does not disclose adhesively bonding two semiconductor chips together, and as a result does not disclose printing electrical lines on main sides of semiconductor chips such that the lines run from contact points of the semiconductor chips beyond lower edges of the main sides onto base sides of the semiconductor chips. However, Henle et al. does disclose printing electrical lines on main sides of semiconductor chips such that the lines run from contact points of the semiconductor chips beyond lower edges of the main sides onto base sides of the semiconductor chips (Fig. 1; col. 3, lines 36-47). Examiner concedes that Henle et al. does not disclose adhesively bonding two semiconductor chips together. However, Kinsman does disclose adhesively bonding two semiconductor chips together (Fig. 1 & 3b; col. 4, lines 52-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Henle et al. by producing a chip composite by adhesively bonding together non-printed main sides of two semiconductor chips as taught by Kinsman to create a device with low impedance (col. 3, lines 11-15).

Applicant also argues Kinsman disclose more than two semiconductor devices are laminated together. However, figures 1, 3, 4, 7 and 10 of Kinsman all disclose two semiconductor devices bonded together (col. 4, lines 52-65). Column 1, lines 22-27 of

Kinsman disclose securing back-to-back mounted semiconductor device perpendicular to a carrier substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Holman et al. (6,005,776) disclose printing electrical lines of main sides of semiconductor chips such that the lines run from contact points of the semiconductor chips beyond lower edges of the main sides onto base sides of the semiconductor chips.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

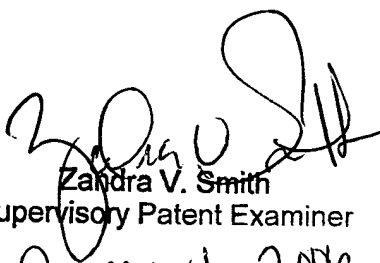
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571)

272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP


Zandra V. Smith
Supervisory Patent Examiner
2 March 2008